being exposed to an outside of a seal member through a side surface thereof;

a second semiconductor chip arranged on said plate member having a fourth plurality of pads;

a first structure and a second structure respectively and electrically inter-connecting said third plurality of pads of said first semiconductor chip with said first plurality of pads of said substrate and said fourth plurality of pads of said second semiconductor chip with said second plurality of pads of said substrate; and

the seal member sealing said first semiconductor chip and said second semiconductor chip.

2. (Amended) A semiconductor device according to claim 1, wherein said structure electrically connecting said third plurality of pads of said first semiconductor chip and said fourth plurality of pads of said second semiconductor chip respectively to said first plurality of pads and said second plurality of pads of said substrate by bonding wires.

5. (Amended) A semiconductor device according to claim 1, wherein said plate member includes a fifth plurality of pads and a sixth plurality of pads, a third structure and a fourth structure respectively and electrically inter-connecting said third plurality of pads of said first semiconductor chip with said first plurality of pads of said substrate and said fourth plurality of pads of said second semiconductor chip with said first plurality of pads of said substrate;

wherein a first member electrically connecting said fourth plurality of pads of said second semiconductor chip with said sixth plurality of pads of said plate member and a second member electrically connecting said fifth plurality of pads plate member with said second plurality of pads

of said substrate.

Q2

6. (Amended) A semiconductor device according to claim 1, wherein said plate member has a first portion covered by said first and second semiconductor chips, and a second portion protruding from said first and second semiconductor chips, said second portion having the side surface of the second end being flush with a side surface of the seal member.

Please add new claim 7 as shown below:

7. (New) A semiconductor device comprising:

a substrate having a first plurality of pads and a second plurality of pads;

a first semiconductor chip mounted on said substrate and having a third plurality of pads;

Q3

a plate member arranged on said first semiconductor chip having a first end at an inward position of said first semiconductor chip adjacent from the third plurality of pads, and a second end being flush with said first semiconductor chip;

a second semiconductor chip arranged on said plate member having a fourth plurality of pads;

a first structure and a second structure respectively and electrically inter-connecting said third plurality of pads of said first semiconductor chip with said first plurality of pads of said substrate and said fourth plurality of pads of said second semiconductor chip with said second plurality of pads of said substrate; and

a seal member sealing said first semiconductor chip and said second semiconductor chip.